LED Packaging: The Largest Opportunity For LED Cost Reduction

18/07/2012

Webcast
Agenda

• Why Cost Reduction of Packaged LED is Required?

• Key Technology Trends in LED Packaging & Associated Players

• Potential Impact of Cost Reduction on LED Value Chain and Markets

• Conclusion
Why Cost Reduction of Packaged LED is Required?
General Lighting
Main Drivers

Total Cost of Ownership (TCO) = Upfront Cost + Energy Cost + Maintenance Cost

Comparison of Average Selling Price (ASP) of different technology of lamp
All sources are ~ 800 lumens, warm White and tier-1 brand only

Incandescent < $1
Fluorescent ~ $3-$5
LED ~ $20-$40

1. Depending on geographical region - Price listed is worldwide average
LED packages represent nearly 30% to 60% off the total cost of LED-based lighting products (depending on the application targeted).
Cost Structure of Packaged LED

Packaging typically accounts for 20% to 50% (~35% in average) of the packaged LED Cost... And represents therefore one of the largest opportunity for cost reduction at the components level...

Source: 2011 DoE Manufacturing Roadmap

Packaged LED Cost Roadmap

Cost Reduction X7

Packaged LED Cost Structure

- Wafer Processing 23%
- Epitaxy 21%
- Substrate 11%
- Phosphor 11%
- Packaging 34%

Source: 2011 Yole Développement

Source: 2011 Yole Développement
Key Technology Trends in LED Packaging & Associated Players
LED Manufacturing Process Flow
Back-End Level (From Epiwafer to Packaged LED)

1. EpiWafer Bonding
   - Carrier wafer
   - Epiwafer

2. Substrate Removal
   - Carrier wafer
   - Epitaxial substrate

3. Wafer Inspection / Defect Mapping

4. Wafer Probing
   (Electrical / Optical)

5. Interconnect

6. Die Attach
   - Die
   - Package Substrate

7. Die Inspection, Testing & Sorting

8. Wafer Backgrinding
   - Die Singulation

9. Phosphor & Encapsulant

10. Lens attach or molding
   - Lens

11. Testing and Sorting

12. Osram Oslon
    Source: Osram

Source: Osram
The Path to Cost Reduction

Consensus → Need for a cost reduction of a factor > 10

\[ \text{COST} = \frac{\text{MANUFACTURING EFFICIENCY} \times 5}{\text{LUMEN} \times (2-3)} \]
10 Key Technologies & Research Areas
Relative Impact on LED Cost of Ownership at Packaging Level

Packaging Design

Wafer Level Packaging
Si-TSV, Wafer level optics

Phosphors
Conversion efficiency, Color Rendering, “IP free” phosphors

Phosphors
Quantum dots phosphors

Thermal Management
New materials for packaging

Current Droop

Testing & Binning
Wafer level, Higher throughputs

Die Singulation
Increased throughputs and yields

Substrate Separation
Laser lift off, Other separation techniques

Encapsulation
Materials and Optics
Ageing and optical properties

Source: Yole Développement
# Details on Die Singulation, Testing & Binning, Substrate Separation, Current Droop and WLP (1/2)

<table>
<thead>
<tr>
<th>Technology / Research Areas</th>
<th>Description</th>
<th>Cost Reduction Opportunities</th>
<th>Associated Players</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die Singulation</strong></td>
<td>2 different types of process are currently used for LED die singulation (Dicing / Scribing &amp; Breaking) → <strong>Critical parameters:</strong> Street width / Cutting speed / Cutting yields / Performance</td>
<td>Improving throughput by increasing speed, reducing street width and / or developing new techniques.</td>
<td>JPSA, QMC, ESI, ALSI, Hamamatsu…</td>
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<tr>
<td><strong>Testing &amp; Binning</strong></td>
<td>Each die and package is tested and sorted for at least 3 parameters (Luminous Flux / Color / Forward Voltage) → <strong>The industry still throws away &gt; 50% of the dies.</strong></td>
<td>Improve testing throughput / accuracy through <strong>improvement in visual inspection for assembly defects, electrical &amp; optical testing, sorting and reliability testing.</strong></td>
<td>Shibuya, Han*s Laser, ESI, Autec…</td>
</tr>
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<tr>
<td>Substrate Separation</td>
<td>Substrate separation technologies are used to bond the epiwafer to a carrier wafer with the desirable properties and removing the initial substrate → Development of vertical LED</td>
<td>Improving performance of LEDs by accessing to new structure more efficient in terms of light extraction.</td>
<td>JPSA, Ushio, QMC, NTT…</td>
</tr>
<tr>
<td>Current Droop</td>
<td>Current droop consists in a decrease of LED efficiency observed when the current density is increased beyond a certain threshold → Various explanations have been suggested but a consensus is yet to be found.</td>
<td>Improving performance of LED by being able to develop 100% droop free LED.</td>
<td>/</td>
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</table>
Details on Phosphors (1/2)

• How to make white light?

Blue Chip + Yellow Phosphor

400 500 600 700nm

UV Chip + 3 Phosphors

400 500 600 700nm

• Key requirements:
  – Excitation and emission wavelength.
  – Conversion efficiency.
  – Cost.
  – Intellectual Property.
  – Stability.
  – Compatibility with encapsulation material.
Details on Phosphors (2/2)

- **Trends:**
  - Development of new materials (→ Quantum Dots), allowing adjustable size / composition to tune absorption and emission wavelengths, and narrowband emission.
  - Development of new Phosphor deposition process (→ Conformal & Preform), allowing highly uniform color, optically homogeneous solid state material, precisely controlled phosphor absorption and tight control of color distribution.
  - Development of Remote Phosphors, allowing better control of phosphor temperature (reduced thermal quenching or shifting), good color homogeneity and tighter control and reproducibility.
Details on Wafer Level Packaging (1/2)

- Wafer Level Packaging consists in packaging several LEDs at wafer level, rather than assembling the package of each individual unit after wafer dicing.

Note: in this example, the LED chips are singulated before being positioned onto the package wafer (=“Chip to Wafer” packaging)

1) Wafer level preparation of the package substrate
2) Chip to wafer
3) Wafer level interconnect, phosphor deposition, encapsulation, optic
4) LED package separation

Overview of Chip to Wafer LED WLP process
Source: Yole Développement
Details on Wafer Level Packaging (2/2)

- **Benefits:**
  - Reliability: Monolithic assembly, Reduced wire interconnect and Good CTE match with GaN
  - Small form factors, ultra-thin, compact packages.
  - Wafer level testing.
  - Reduced cost: wafer level manufacturing.
Details on Thermal Management

- For LED, up to 40% of the energy turned into heat...
- ... However, LED DON’T like heat → Decrease of performance (Brightness, Efficiency / Lifetime...).
- Trends:

```
LED Die

<table>
<thead>
<tr>
<th>Chip on Board</th>
<th>Substrate Only</th>
<th>Si Submount</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Heat slug</td>
<td>Heat slug</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ceramic</td>
<td>Ceramic</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Silicon (Wafer Level)</td>
<td>Viscera Technology</td>
<td></td>
</tr>
<tr>
<td>PCB</td>
<td>Optek Lednium</td>
<td>Lumileds Luxeon Rebel</td>
<td>Lumileds Luxeon</td>
</tr>
<tr>
<td></td>
<td>Ceramic</td>
<td>Ceramic</td>
<td>Cree-X-lamp</td>
</tr>
<tr>
<td>PCB (MCPCB, FR-4, CEM-3, Ceramic...)</td>
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Details on Encapsulation Materials and Optics

- **Main requirements:**
  - Non-yellowing / Durability.
  - Good refractive index.
  - Good thermo-mechanical properties.
  - High and low temperature resistance.
  - Good adhesion.
  - Non-porous.
  - Low cost.

- **Trends:**

<table>
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<tr>
<th>Process</th>
<th>Materials</th>
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<tbody>
<tr>
<td>Potting</td>
<td>Acrylcs</td>
</tr>
<tr>
<td>Printing</td>
<td>Silicon</td>
</tr>
<tr>
<td>Molding (Transfer, Injection, compression)</td>
<td>Polycarbonates</td>
</tr>
<tr>
<td>Wafer Level Replication</td>
<td>Cyclo Olefin Copolymer</td>
</tr>
</tbody>
</table>
## Details on Packaging Design (1/2)

<table>
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<tr>
<th>Middle Power</th>
<th>Single Large Die</th>
<th>Multiple Large Die</th>
<th>Small / Medium COB Array</th>
<th>Single or Multi “Jumbo Die”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lumileds</td>
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<td>Cree</td>
<td>Edison Opto</td>
<td>Luminus Device</td>
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</table>

- **Single Large Die**: Lumileds
- **Multiple Large Die**: Cree
- **Small / Medium COB Array**: Edison Opto
- **Single or Multi “Jumbo Die”**: Luminus Device

**Diagram**:
- Single Die x 10
- Multi Die x 24
- COB (Single Die)
Details on Packaging Design (2/2)

**Small Die or Large Chips:**

<table>
<thead>
<tr>
<th>Small Chips Benefits</th>
<th>Higher binning yields / Increased thermal management (distributed heat load) / High Voltage packages</th>
</tr>
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<tr>
<td>Small Chips Drawbacks</td>
<td>Packaging complexity / Beam shaping / Larger package volume</td>
</tr>
</tbody>
</table>

**Standardization can reduce cost**

- Lighting applications require high power packages, right?...
- ... Mid-power LED have price decreased dramatically in 2011 under the combined effects of “Package Standardization + Very large volumes + High level of competition (over supply)” → Highly competitive $/lumen ratio.

→ Middle power packages crossing over from display to lighting!!!

2 Chip 5630 packages
Source: Seoul Semiconductor
Potential Impact of Cost Reduction on LED Value Chain and Markets
LED Lighting Value Chain Overview

- Assembly of LED package(s) on Printed Circuit Board (PCB)
- Integration of optic, heat sink / thermal management, IC driver / power supply and case

Material / Substrate

- Growth of epilayer on wafer
- Structuration and doping of the substrate

Die / Chip

- Encapsulation and realization of contact
- Add of thermal management
- Coating with phosphor (for white LED)

Packaged LED

Module / Light Engine

Lamp

Lighting Fixture

System / Solution

- Combination of module and ballast with a fixture (additional optic, heat sink and case)

- Enhancement of the lighting fixture by attaching external lighting control units

- Combination of module with additional optic, heat sink and case

Distributors

Consumers
LED Lighting Value Chain
Impact of Cost Reduction - “Display Application” Model

Commoditization / Standardization
- Commoditization of chip manufacturing.
- New entrants should professionalize the epitaxy process.

Value Transfer
- Add of functionalities
- New Asian players should enter the business, especially for low- and middle-end applications. Despite commoditization, profit can keep high with high-end applications.

Integration
- Add of functionalities
- New designing of fixtures and improvement of system size should increase margin.

Vertical Integration
Consolidation
Conclusion
Conclusion

More than x6 cost reduction in packaged LEDs cost?
Not easy but achievable through combination of different parameters

- Technology improvements: efficiency + more lumens per chip.
- Manufacturing improvements: dedicated LED tools, automation, inline testing.
- Economies of scale
- Higher integration
- Standardization

LED industry maturing and reaching critical mass to enable development of dedicated tools. Semiconductor “veteran” companies bring additional expertise and “best practices”.