LED Packaging: The Largest Opportunity For LED Cost Reduction

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Webcast

75 cours Emile Zola, F-69001 Lyon-Villeurbanne, France
Tel : +33 472 83 01 80 - Fax : +33 472 83 01 83
Web: http://www.yole.fr

Agenda

- Why Cost Reduction of Packaged LED is Required?
- Key Technology Trends in LED Packaging & Associated Players
- Potential Impact of Cost Reduction on LED Value Chain and Markets
- Conclusion

Why Cost Reduction of Packaged LED is Required?

General Lighting
Main Drivers

Total Cost of Ownership (TCO) =

- **Upfront Cost**
- \+
- **Energy Cost**
- \+
- **Maintenance Cost**



Upfront Cost

Comparison of Average Selling Price (ASP) of different technology of lamp
All sources are ~ 800 lumens, warm White and tier-1 brand only


Incandescent
< $1

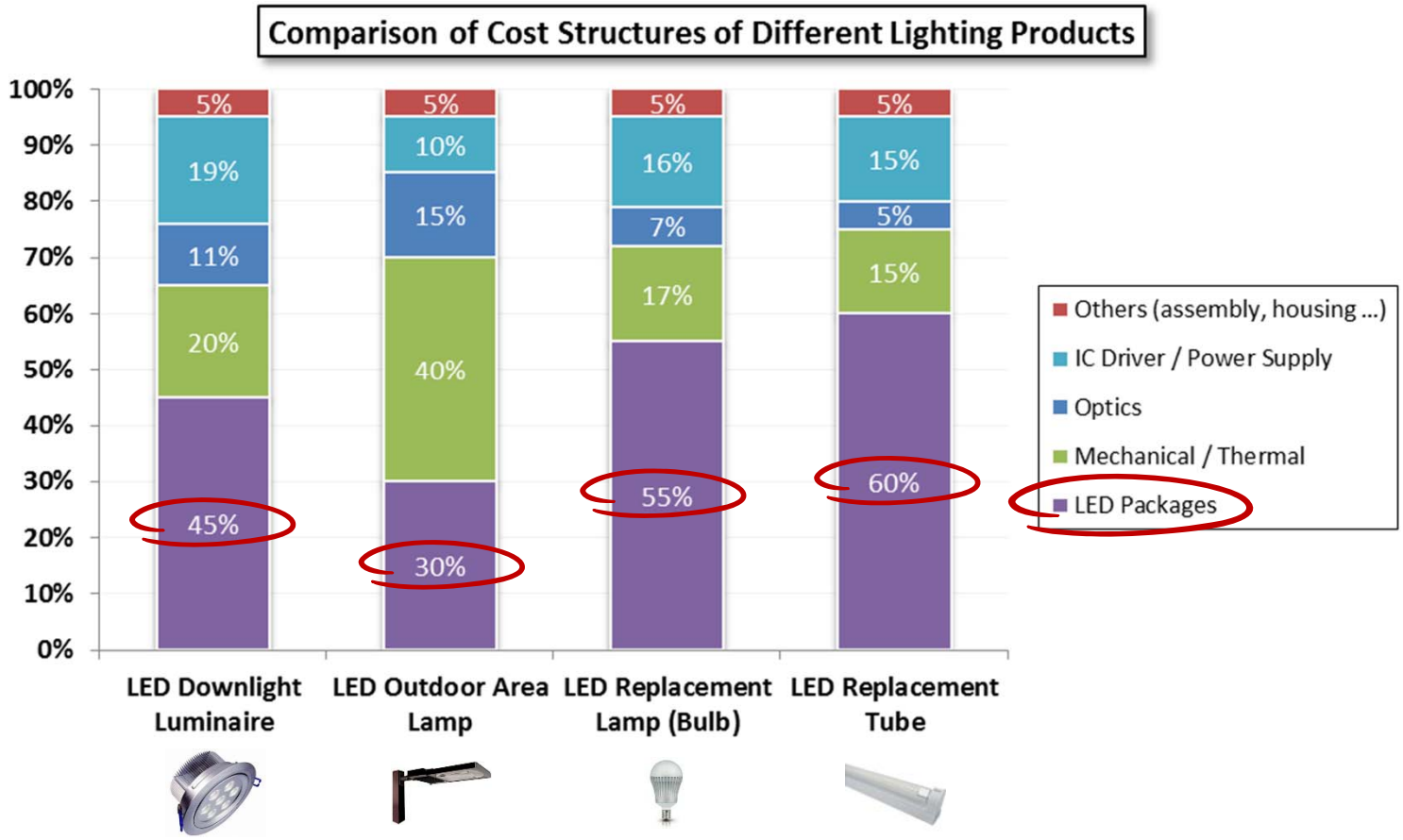
Fluorescent
~ $3-$5

LED
~ $20-$40[1]

1. Depending on geographical region - Price listed is worldwide average

General Lighting
Typical Cost Structure of Lighting Products

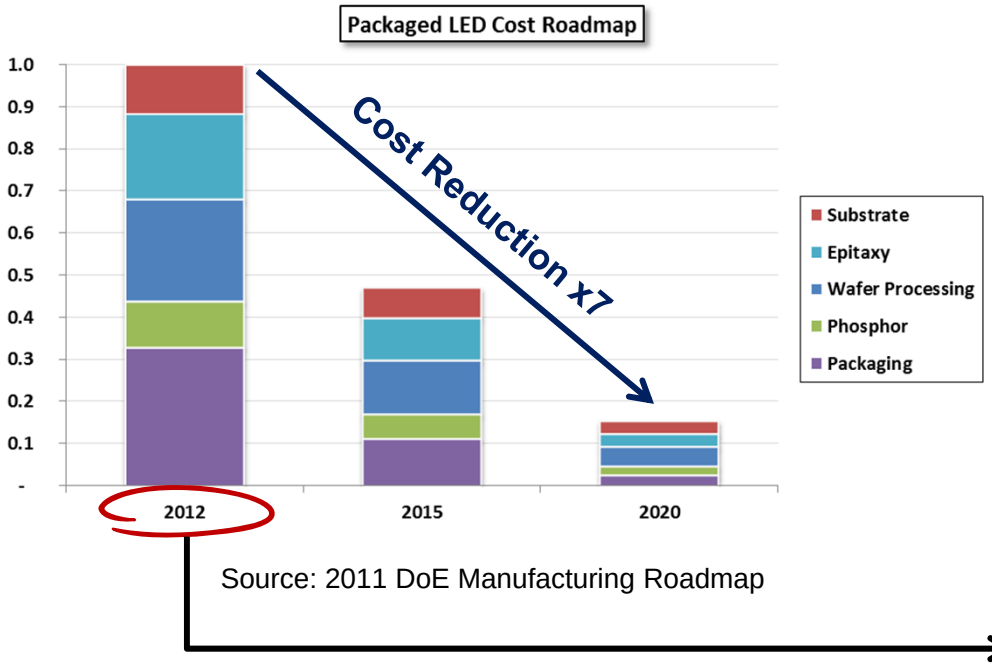
LED packages represent nearly 30% to 60% off the total cost of LED-based lighting products (depending on the application targeted).



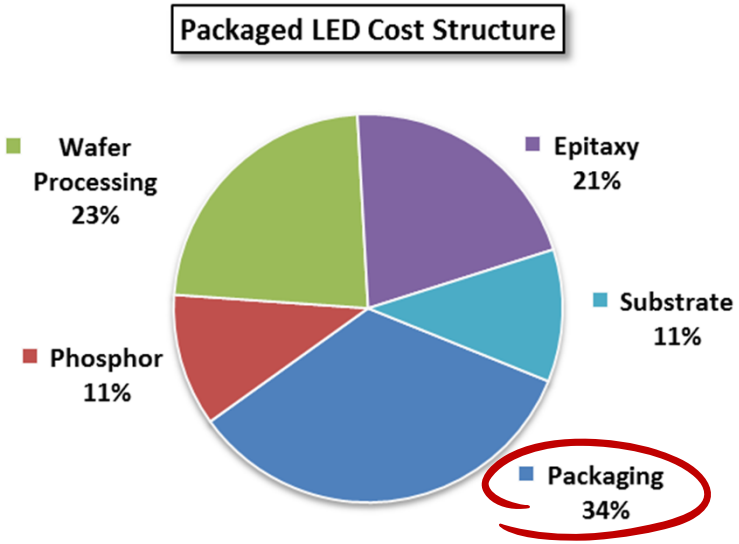
Source: 2011 DoE Manufacturing Roadmap - Yole Développement

Cost Structure of Packaged LED

Packaging typically accounts for 20% to 50% (~35% in average) of the packaged LED Cost… And represents therefore one of the largest opportunity for cost reduction at the components level…



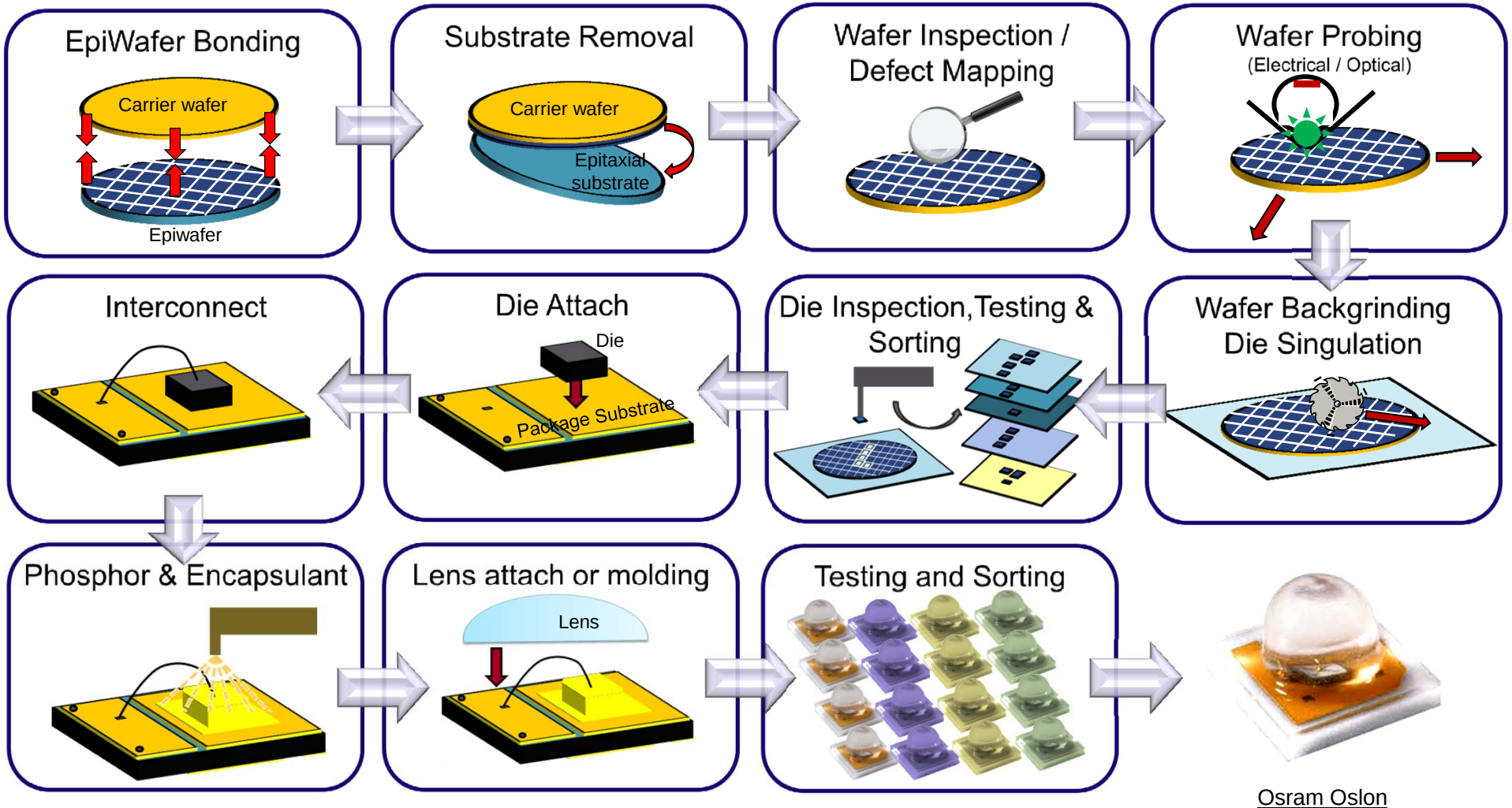
Source: 2011 DoE Manufacturing Roadmap



Source: 2011 Yole Développement

Key Technology Trends in LED Packaging & Associated Players

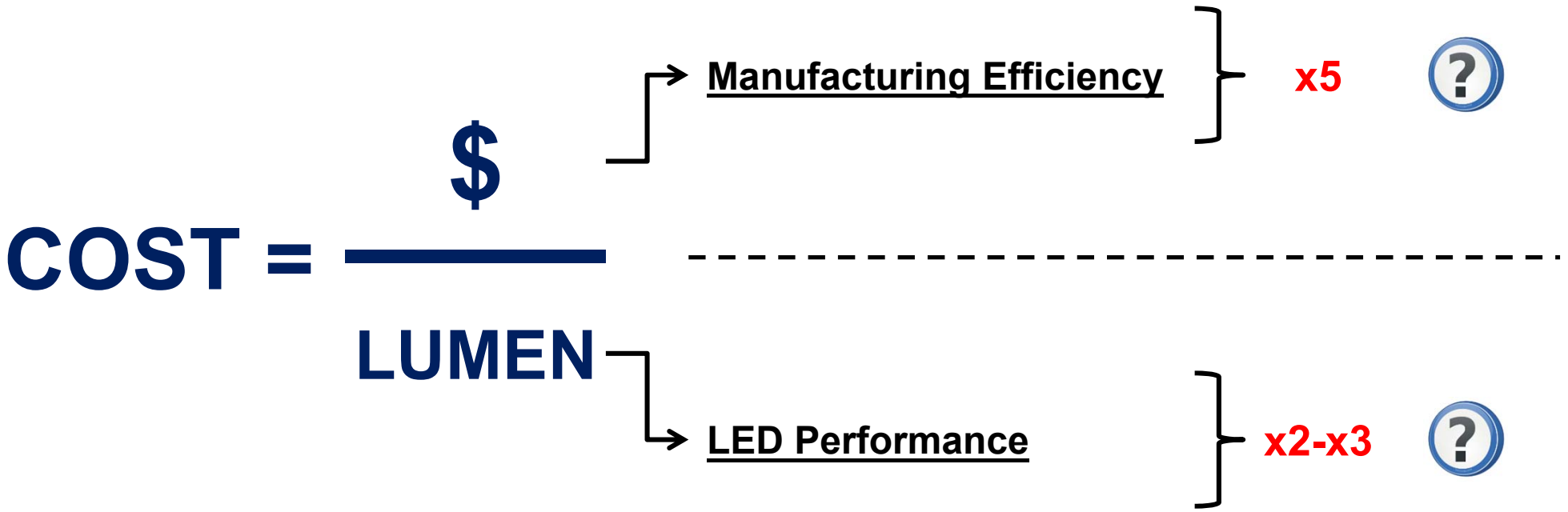
LED Manufacturing Process Flow
Back-End Level (From Epiwafer to Packaged LED)



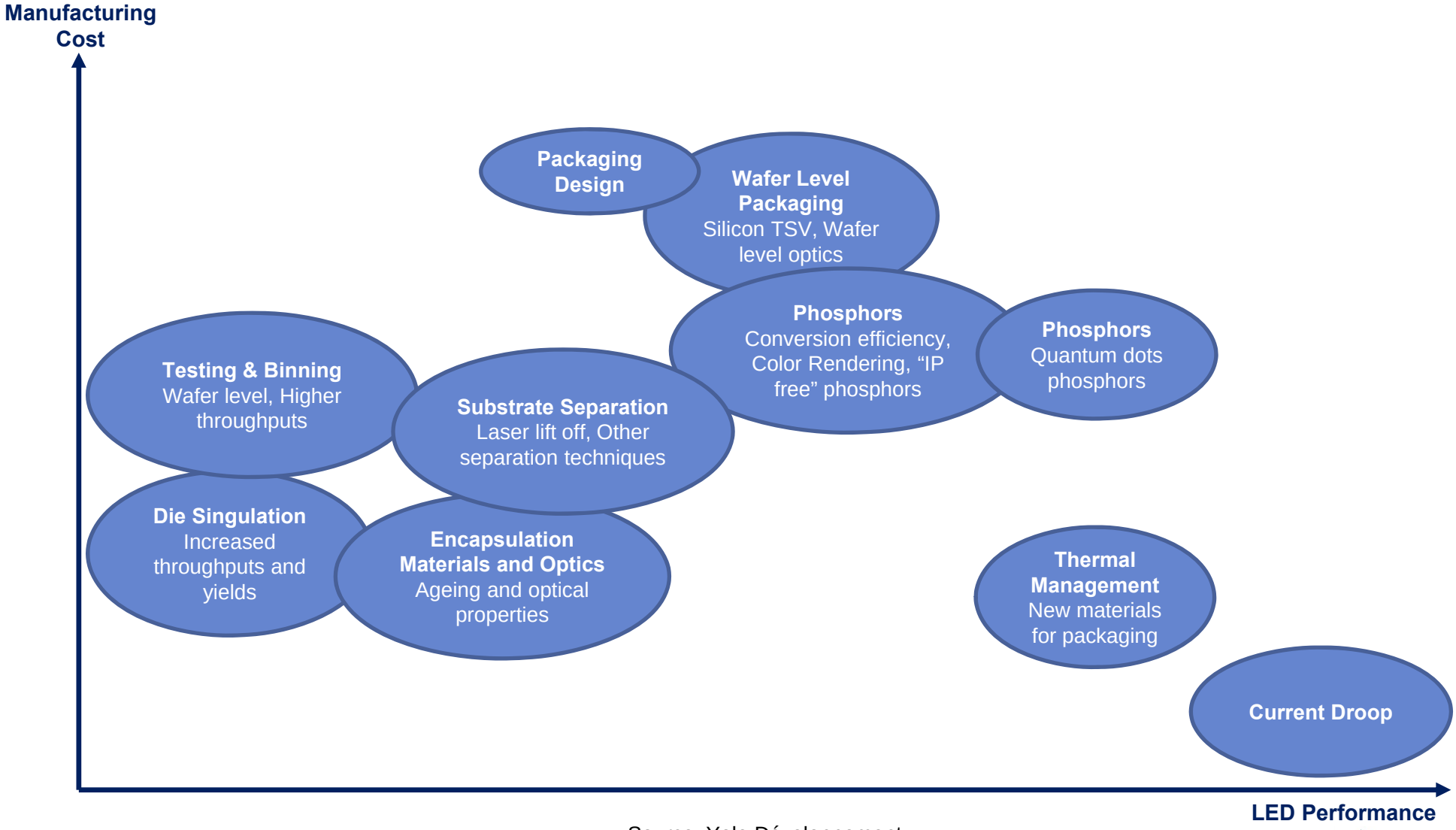
Osram Oslon
Source: Osram

The Path to Cost Reduction

Consensus → Need for a cost reduction of a factor > 10



10 Key Technologies & Research Areas
Relative Impact on LED Cost of Ownership at Packaging Level



Source: Yole Développement

Details on Die Singulation, Testing & Binning, Substrate Separation, Current Droop and WLP (1/2)

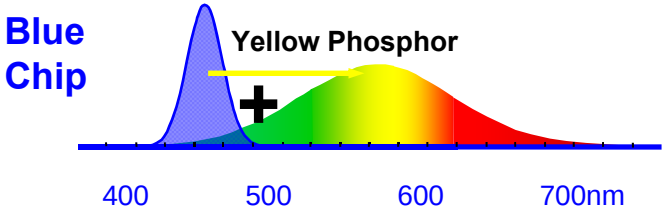
Technology / Research Areas	Description	Cost Reduction Opportunities	Associated Players
Die Singulation	2 different types of process are currently used for LED die singulation (Dicing / Scribing & Breaking) → **Critical parameters: Street width / Cutting speed / Cutting yields / Performance**	Improving throughput **by increasing speed, reducing street width and / or developing new techniques**.	*JPSA, QMC, ESI, ALSI, Hamamatsu…*
Testing & Binning	Each die and package is tested and sorted for at least 3 parameters (Luminous Flux / Color / Forward Voltage) → **The industry still throws away > 50% of the dies**.	Improve testing throughput / accuracy through **improvement in visual inspection for assembly defects, electrical & optical testing, sorting and reliability testing**.	*Shibuya, Han*s Laser, ESI, Autec…*

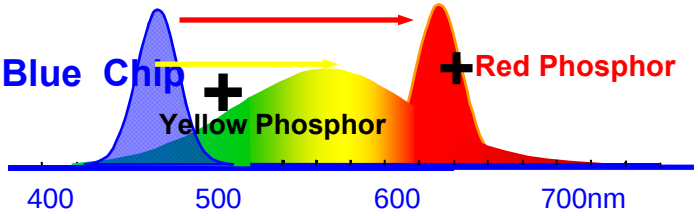
Details on Die Singulation, Testing & Binning, Substrate Separation, Current Droop and WLP (2/2)

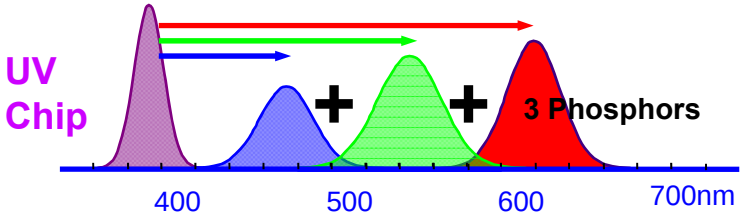
Technology / Research Areas	Description	Cost Reduction Opportunities	Associated Players
Substrate Separation	Substrate separation technologies are used to bond the epiwafer to a carrier wafer with the desirable properties and removing the initial substrate → **Development of vertical LED**	Improving performance of LEDs **by accessing to new structure more efficient in terms of light extraction**.	*JPSA, Ushio, QMC, NTT…*
Current Droop	Current droop consists in a decrease of LED efficiency observed when the current density is increased beyond a certain threshold → **Various explanations have been suggested but a consensus is yet to be found.**	Improving performance of LED **by being able to develop 100% droop free LED**.	/

Details on Phosphors (1/2)

- **How to make white light?**



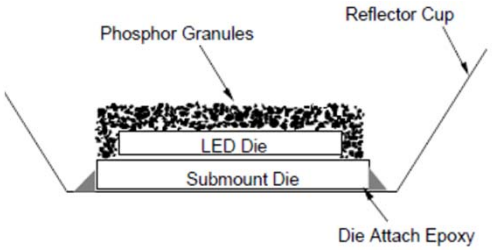




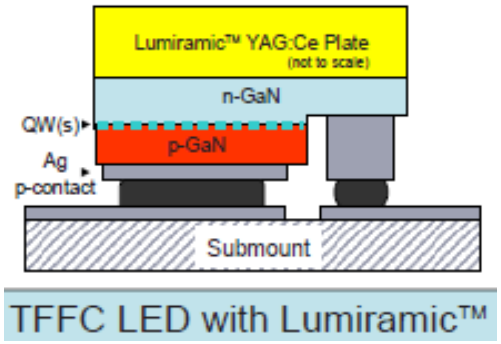
- **Key requirements:**
  - **Excitation and emission wavelength.**
  - **Conversion efficiency.**
  - **Cost.**
  - **Intellectual Property.**
  - **Stability.**
  - **Compatibility with encapsulation material.**

Details on Phosphors (2/2)

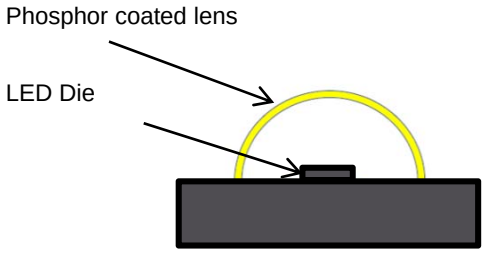
- **Trends:**
  - **Development of new materials (→ Quantum Dots), allowing adjustable size / composition to tune absorption and emission wavelengths, and narrowband emission.**
  - **Development of new Phosphor deposition process (→ Conformal & Preform), allowing highly uniform color, optically homogeneous solid state material, precisely controlled phosphor absorption and tight control of color distribution.**
  - **Development of Remote Phosphors, allowing better control of phosphor temperature (reduced thermal quenching or shifting), good color homogeneity and tighter control and reproducibility.**



Conformal Phosphor Deposition Process



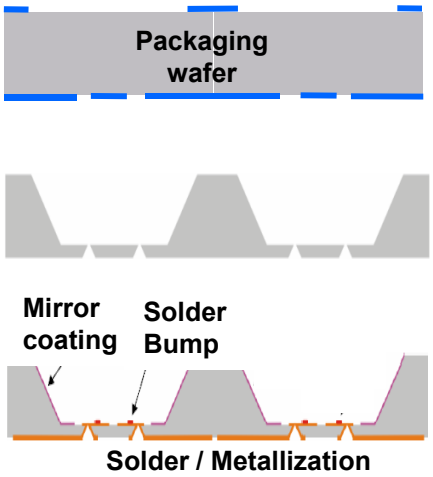
Preform Phosphor Deposition Process



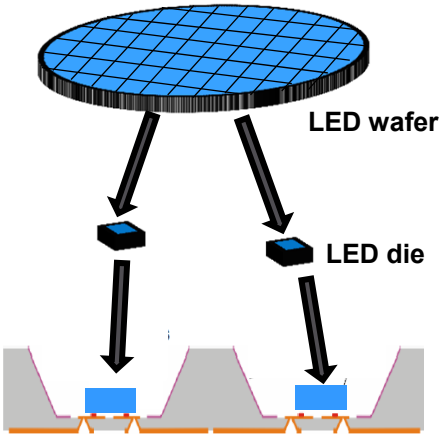
Remote Phosphor

Details on Wafer Level Packaging (1/2)

- **Wafer Level Packaging consists in packaging several LEDs at wafer level, rather than assembling the package of each individual unit after wafer dicing.**

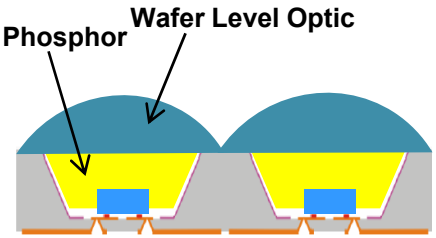


1) Wafer level preparation of the package substrate

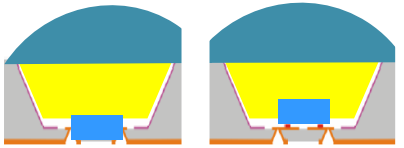


2) Chip to wafer

Note: in this example, the LED chips are singulated before being positioned onto the package wafer (="Chip to Wafer" packaging)



3) Wafer level interconnect, phosphor deposition, encapsulation, optic



4) LED package separation

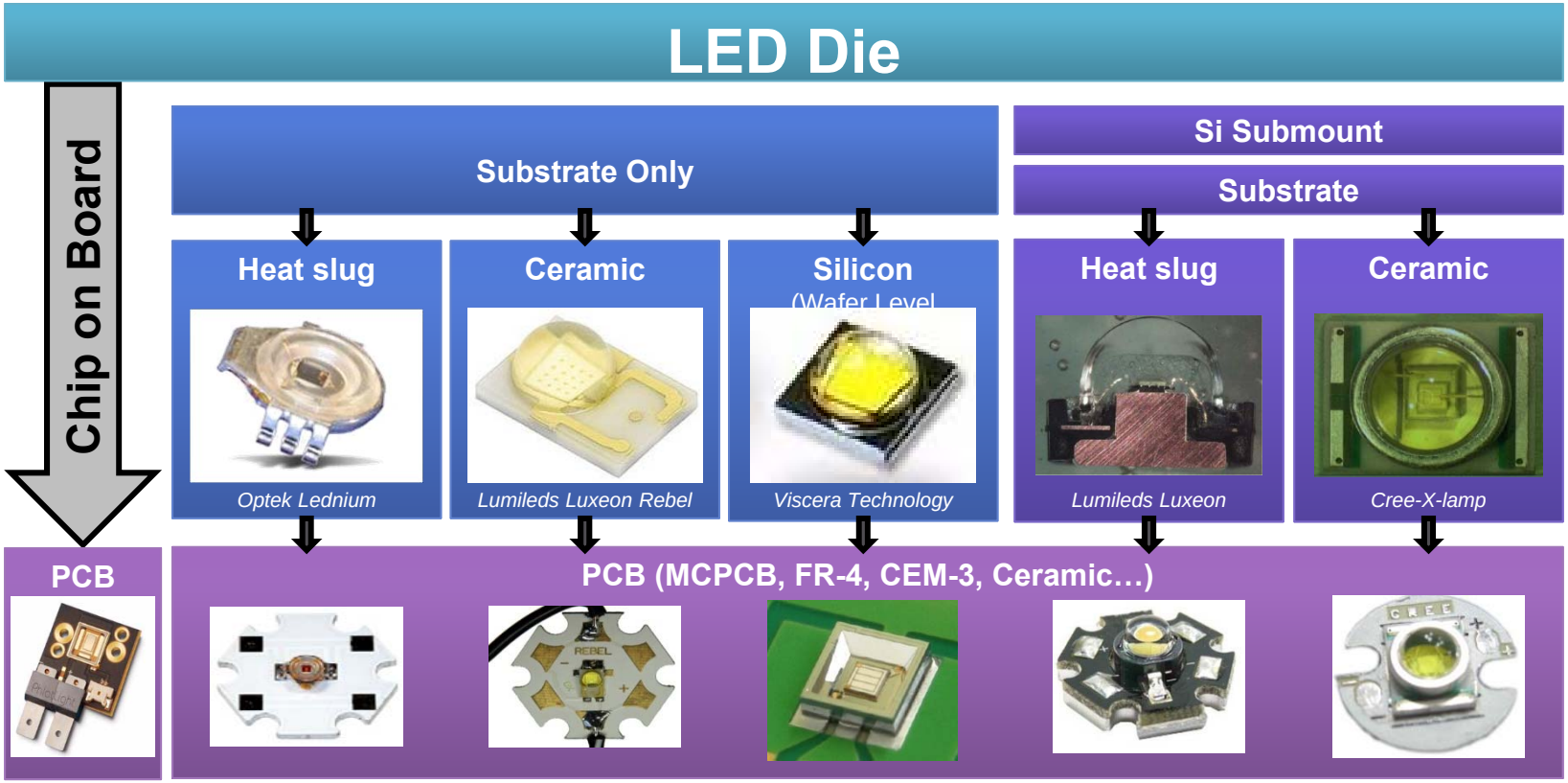
Overview of Chip to Wafer LED WLP process
Source: Yole Développement

Details on Wafer Level Packaging (2/2)

- **Benefits:**
  - **Reliability: Monolithic assembly, Reduced wire interconnect and Good CTE match with GaN**
  - **Small form factors, ultra-thin, compact packages.**
  - **Wafer level testing.**
  - **Reduced cost: wafer level manufacturing.**

Details on Thermal Management

- For LED, up to 40% of the energy turned into heat…
- … However, LED **DON'T** like heat → Decrease of performance (Brightness, Efficiency / Lifetime…).
- Trends:

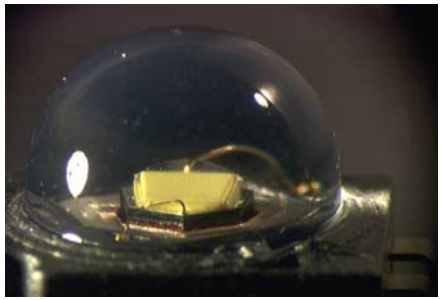


Details on Encapsulation Materials and Optics

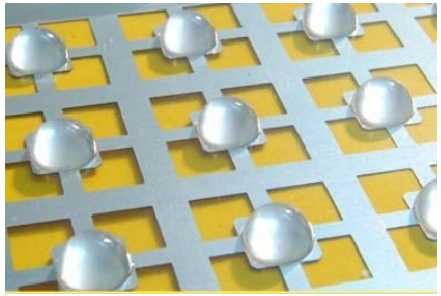
- **Main requirements:**
  - **Non-yellowing / Durability.**
  - **Good refractive index .**
  - **Good thermo-mechanical properties.**
  - **High and low temperature resistance.**
  - **Good adhesion.**
  - **Non-porous.**
  - **Low cost.**

- **Trends:**

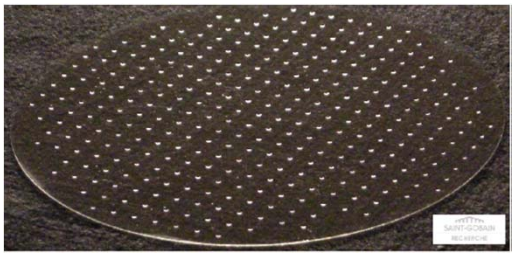
Process	Materials
Potting	Acrylics
Printing	Silicon
Molding (Transfer, Injection, compression)	Polycarbonates
Wafer Level Replication	Cyclo Olefin Copolymer



Luxeon K2
Source: Mu Analysis

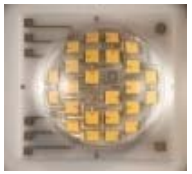


Lens by compression molding on lead frames
Source: ASM Pacific Technology

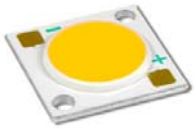


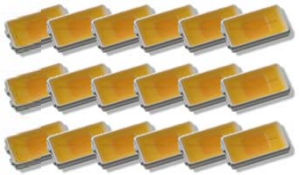
Gradient Index Flat Glass Wafer

Details on Packaging Design (1/2)

Middle Power	Single Large Die	Multiple Large Die	Small / Medium COB Array	Single or Multi "Jumbo Die"
				
Lumileds	*Lumileds*	*Cree*	*Edison Opto*	*Luminus Device*

- COB (Single Die)
- Single Die x 10
- Multi Die x 24





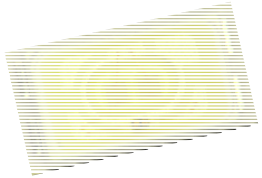
Details on Packaging Design (2/2)

- **Small Die or Large Chips:**

Small Chips Benefits	Higher binning yields / Increased thermal management (distributed heat load) / High Voltage packages
Small Chips Drawbacks	Packaging complexity / Beam shaping / Larger package volume

- **Standardization can reduce cost**
  - **Lighting applications require high power packages, right?…**
  - **… Mid-power LED have price decreased dramatically in 2011 under the combined effects of "Package Standardization + Very large volumes + High level of competition (over supply)" → Highly competitive $/lumen ratio.**

→ Middle power packages crossing over from display to lighting!!!



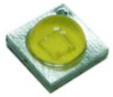
2 Chip 5630 packages
Source: Seoul Semiconductor

Potential Impact of Cost Reduction on LED Value Chain and Markets

LED Lighting Value Chain
Overview

- Assembly of LED package(s) on Printed Circuit Board (PCB)
- Integration of optic, heat sink / thermal management, IC driver / power supply and case

- Growth of epilayer on wafer
- Structuration and doping of the substrate

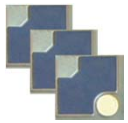


- Combination of module and ballast with a fixture (additional optic, heat sink and case)

Material / Substrate → Die / Chip → Packaged LED → Module / Light Engine → Lamp → Lighting Fixture → *System / Solution*

Distributors

Consumers

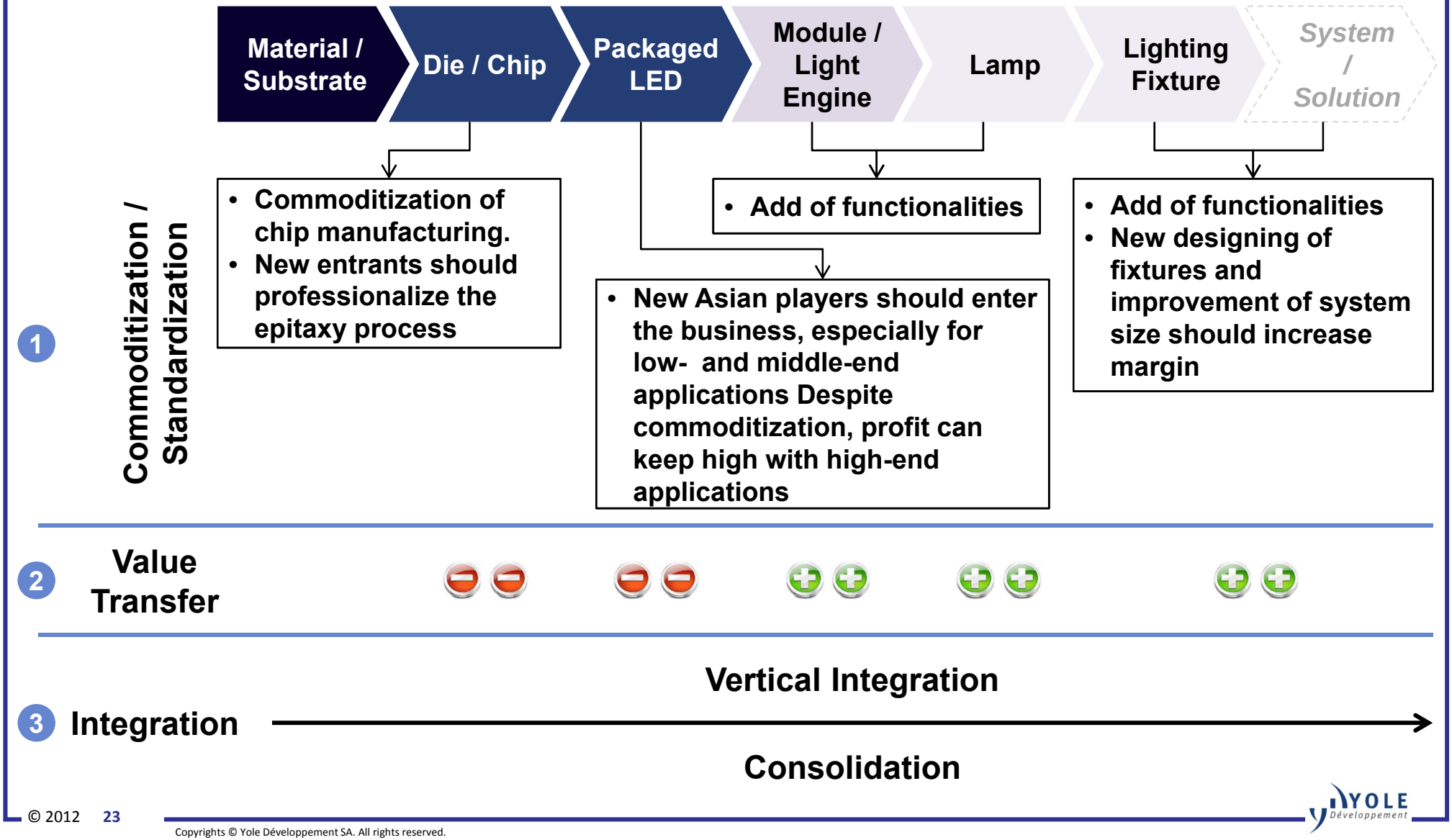


- Encapsulation and realization of contact
- Add of thermal management
- Coating with phosphor (for white LED)

- Enhancement of the lighting fixture by attaching external lighting control units

- Combination of module with additional optic, heat sink and case

LED Lighting Value Chain
Impact of Cost Reduction - "Display Application" Model



Conclusion

Conclusion

More than x6 cost reduction in packaged LEDs cost?

Not easy but achievable through combination of different parameters

- Technology improvements: efficiency + more lumens per chip.
- Manufacturing improvements: dedicated LED tools, automation, inline testing.
- Economies of scale
- Higher integration
- Standardization

LED industry maturing and reaching critical mass to enable development of dedicated tools. Semiconductor "veteran" companies bring additional expertise and "best practices".