Thin Wafers Bonding & Processing

A market perspective
Why New Handling Technologies

- Consumer electronics is today a big driver for smaller, higher performing & lower cost device configurations.

- These new options, in turn, are pushing demand for thin (< 100 µm) and even ultra-thin semiconductor wafers (< 40µm) for:
  - Reduced thickness and package
  - Better heat dissipation for thermal management
  - Increased TSV density

- But as wafer thickness decreases to 100µm and below, manufacturing challenges arise:
  - Wafers are less stable
  - Wafers are more vulnerable to stress
  - Dies can warp & break

→ Special thin wafer handling processes (such as temporary bonding) are thus necessary.
Thin Wafer Applications

- HBLEDs
- Interposers
- Photovoltaic
- Power Devices
- RF
- CMOS Image Sensors
- MEMS

3D Stacking of memory, logic
### Thin Wafer Roadmap

**TODAY (2012)**

- **MEMS substrates**: 500-100µ
- **MEMS capping**: 100-300µ
- **ASIC MEMS**: 100-150µ
- **CIS Packaging**: 200µ
- **CIS BSI**: <10µ
- **Memories**: 100-150µ
- **Logic**: 300µ
- **Power Devices**: 75µ
- **RF Devices**: 300µ
- **LEDs**: 100µ
- **PV**: 180-200µ

**TOMORROW (2017)**

- **MEMS substrate**: 150µ
- **MEMS capping**: 50µ
- **ASIC MEMS**: 100µ
- **CIS Packaging**: 75µ
- **CIS BSI**: 3µ
- **Memories**: 25µ
- **Logic**: 200µ
- **Power Devices**: 30µ
- **RF Devices**: 50µ
- **LEDs**: 80µ
- **PV**: 140-160µ
By 2017, we estimate the ratio of THIN wafers vs. TOTAL number of wafers (in 300 mm eq.) to be 74%.
• Memory and logic wafers account for the largest segment of thin wafer shipments: in 2017, we estimate the ratio to be 76%.
12” wafers will account for the largest share of thin wafers (memory & logic application).

By 2017, it will be 56% of total thin wafers (in units).

### Thin wafers forecast 2011-2017 in kunits

<table>
<thead>
<tr>
<th>Year</th>
<th>12”</th>
<th>8”</th>
<th>6”</th>
<th>5”</th>
<th>4”</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>21 665</td>
<td>4 415</td>
<td>10 611</td>
<td>2 210</td>
<td>16 878</td>
</tr>
<tr>
<td>2012</td>
<td>26 712</td>
<td>4 909</td>
<td>12 477</td>
<td>1 882</td>
<td>18 055</td>
</tr>
<tr>
<td>2013</td>
<td>32 623</td>
<td>5 736</td>
<td>15 278</td>
<td>1 603</td>
<td>17 917</td>
</tr>
<tr>
<td>2014</td>
<td>41 714</td>
<td>6 806</td>
<td>17 455</td>
<td>1 366</td>
<td>17 757</td>
</tr>
<tr>
<td>2015</td>
<td>53 032</td>
<td>7 883</td>
<td>19 478</td>
<td>1 121</td>
<td>18 854</td>
</tr>
<tr>
<td>2016</td>
<td>66 003</td>
<td>9 009</td>
<td>22 543</td>
<td>920</td>
<td>18 629</td>
</tr>
<tr>
<td>2017</td>
<td>71 875</td>
<td>10 881</td>
<td>25 186</td>
<td>755</td>
<td>19 192</td>
</tr>
</tbody>
</table>

**CAGR**
- **22%**
- **16%**
- **15%**
- **-16%**
- **2%**
2011 Wafer Size Breakdown by Wafer Thickness
Percentage in number of wafers

2011 wafer shipment by wafer size/thickness

<table>
<thead>
<tr>
<th>Wafer Size</th>
<th>&lt;10µ</th>
<th>10-99µ</th>
<th>100-199µ</th>
<th>200µ+</th>
</tr>
</thead>
<tbody>
<tr>
<td>12&quot;</td>
<td>306</td>
<td>11 104</td>
<td>0</td>
<td>10 255</td>
</tr>
<tr>
<td>8&quot;</td>
<td>0</td>
<td>1 413</td>
<td>639</td>
<td>2 362</td>
</tr>
<tr>
<td>6&quot;</td>
<td>0</td>
<td>7 110</td>
<td>1 694</td>
<td>1 806</td>
</tr>
<tr>
<td>&lt; 5&quot;</td>
<td>0</td>
<td>18 763</td>
<td>0</td>
<td>325</td>
</tr>
</tbody>
</table>

TOT ~2,334k
TOT ~306k
TOT ~2,334k
TOT ~14,749k
# 2017 Wafer Size Breakdown by Wafer Thickness

Percentage in number of wafers

## 2017 wafer shipment by wafer size/thickness

<table>
<thead>
<tr>
<th>Wafer Size (Inches)</th>
<th>&lt;10µm</th>
<th>10-99µm</th>
<th>100-199µm</th>
<th>200+µm</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>12&quot;</td>
<td>2,158</td>
<td>52,972</td>
<td>0</td>
<td>16,745</td>
<td>103,447k</td>
</tr>
<tr>
<td>8&quot;</td>
<td>0</td>
<td>8,411</td>
<td>2,470</td>
<td>0</td>
<td>16,745k</td>
</tr>
<tr>
<td>6&quot;</td>
<td>0</td>
<td>22,117</td>
<td>3,069</td>
<td>0</td>
<td>16,745k</td>
</tr>
<tr>
<td>&lt;5&quot;</td>
<td>0</td>
<td>19,947</td>
<td>0</td>
<td>0</td>
<td>16,745k</td>
</tr>
</tbody>
</table>

- **TOT ~103,447k**
- **TOT ~2,158k**
- **TOT ~5,539k**
- **TOT ~16,745k**
## Thin Wafer Processors Production Volume

(> 10k WSPY)

<table>
<thead>
<tr>
<th>&gt; 1M WSPY</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 50k WSPY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&gt; 100k WSPY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>500k WSPY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100k WSPY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt; 50k WSPY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**MEMORIES**

- Samsung
- Micron
- Nichia

**LEDs**

- Toshiba
- Sharp
- Everlight

**MEMS**

- Infineon
- Xintec

**POWER**

- ST
- Infineon
- STMicroelectronics

**3D WLCSP**

- Bosch
- Renesas
- Avago

**3DIC**

- TSMC
- Sony
- IBM

**INTERPOSERS**

- Avago
- TSMC
- Samsung

*Images of companies logos are used for each category.*

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Example 1
Discera generation comparison - Temporary bonding is now used

- There are major differences between both generations:
  1. TSV connection from the bottom
  2. Si fusion bonding (instead of glass frit with seal ring ~200µ) 
  3. Temporary bonding step for TSV wafer thinned down 106µ

- The difference between 1st and 2nd generation comes from the interconnection method of the resonator:
  - 1st generation: connection from the side (Manufacturing made by Dalsa)
  - 2nd generation: connection from the bottom (Manufacturing made by Silex Microsystems)
Example 2
Power Semiconductor Devices

PIN Diode
Schottky diode
Power MOSFET
FET
IGBT
BJT
Thyristor: TRIACS

- PIN Diode: No thin wafer
- Schottky diode: No thin wafer
- Power MOSFET: Thin wafer required
- FET: Thin wafer required
- IGBT: Thin wafer required (but R&D only 2012)
- BJT: No thin wafer
- Thyristor: TRIACS: No thin wafer

IGBT has been developed to combine the advantages of both power MOSFET and BJT.
Thin Wafer for Power at Renesas

- Trench-filling epitaxial technology, ultra-thin wafer process technology and space-saving packaging yield more compact systems with high efficiency
Example 3
Thinning, an Enabling Technology for 3D ICs

Wafer technology:
- **Substrate**: Silicon, SOI?
- **Thinning**: Grinding, CMP and plasma technologies...
- **Handling**: how to handle wafers/dies as thin as 15 µm? Is a hard wafer carrier solution is required?

Thickness Budget < 1 mm

**New materials:**
- High viscosity underfiller
- Thermal management
- New dielectrics

**Substrate interposer:**
- Silicon interposers?
- Embedded components & passives?

3D Vias making:
- **Drilling**: Laser or DRIE? Profile control, high etch rates
- **Filling**: Cu, W, PolySi, conductive polymers...
- **Coating**: conformal coatings for seed layers, film isolation...
- **Electroplating** speed requirements to meet

Via last (in BE) or Via first (in FE)?
Via specifications depend on application:
- **Diameters**: from 5 to 100 µm
- **Depth**: from 10 to 100 µm
- **Via densities**: from $10^2$ to $>10^5$ holes / chip

Bonding technology:
- **Technology**: Metal Thermo compression, Direct Oxide ($\text{SiO}_2$), Adhesive bonding...
- **Integration scheme**: C2C, C2W or W2W? Face to face or face to back? YIELD & TEST issues
- **Accuracy**: high throughput C2W equipment is required to bond at ±1 µm accuracies
- **How many dies to stack?**
Why Temporary Bonding?

Temporary (de-)bonding drivers

- Thinning and back side processing of wafers: vertical integration
- High topography wafers
- Double-side processed
- Handling delicate thin wafer

Advanced Packaging
- 3D stacking: High density of integration
- Reduced package size (< 100µm)
- TSV pitch & diameters
- Aspect ratio drives wafer thickness

MEMS
- Reduce total package size of the device
- Protect front side structure for wafers that are double-side processed

Power devices
- Reduced resistance
- Functional integration increased

RF devices
Applications of Bonding / Debonding for Wafer Level Packaging

Wafer-Scale Applications / Platforms

**Wafer-Level Electrical Redistribution**
- WL-CSP 'Fan-in'
- FO-WLP

**Wafer-Level Interface / Encapsulation**
- Capping
- Optics
- Fluidic

**Flip-chip & Wafer-Level Stacking / Integration**
- Embedded IC in PCB
- 3D IC / TSV
- Si on Si flip-chip
- fcBGA

- Only debonding from metal carriers (eWLB by Infineon) as of 2011
- 3D capping and packaging with TSV
- Permanent bonding for CIS and MEMS Packaging
- Temporary bonding and de-bonding

*Thin Wafer Handling Needed*
Thin Wafer Handling Solutions

Thin wafer handling

With carrier

With intermediate layer

Temporary bonding/debonding

Without intermediate layer

Mobile Electro Static Wafer

Without carrier

Adhesive tape

Peripheral Ring

With intermediate layer

With carrier

Without carrier

Materials
- 3M
- TOK
- Brewer Science
- Lintec
- Nitta Haas
- Nitto Denko
- Promerus
- Shin Etsu
- JSR
- Thin Materials AG

Equipment
- EVG
- SUSS MicroTEC
- TEL
- TOK
- 3M
- AML

Carriers/Equipment
- FhG/ProTec
- ProTec/ProTec

Equipment & materials
- TOK
- 3M

Adhesive tape
- Nitto denko
- Lintec

Peripheral Ring

Disco (TAIKO process)
- DoubleCheck
- Semitool (AMAT)
Temporary Bonding
Processes & tools

**Equipment**
- Spin coater
- Bake plate
- Aligner
- Temporary bonder
- Thinning systems
- Inspection systems

**Bonding process/ Carrier**
- Si/Glass
- Glass
- Si/Glass
- Glass
- Si/Glass
- UV light
- Glass

**Equipment**
- Brewer Science (BSI)
- Dupont
- TMAT
- TOK
- ZoneBond (BSI)
- WSS (3M)

**Processes**
- Spin coater adhesive
- Wafer bonding
- Device wafer with adhesive
- Bake + batch cure
- Spin coater adhesive
- Device wafer coated with adhesive
- Spin coater adhesive
- Device wafer coated with adhesive
- Carrier wafer with zones
- Spin coater adhesive
- Device wafer coated with adhesive
- Spin coater adhesive
- Device wafer coated with adhesive
- UV light
Debonding Processes & tools

Debonding processes

- **Thermal Slide-off**
- **Mechanical release with tape frame**
- **YAG Laser with tape frame**
- **Excimer Laser with tape frame**
- **Chemical (solvent) release**

Equipment

- **Thermo-slide debonder**
- **Cleaning system**
- **Frame mounted wafer**
- **Debonder cluster**
- **Cleaning system for the device wafer**
- **Frame mounted wafer**
- **Debonder cluster**
- **Cleaning system for the device wafer**
- **Debonder system**
- **Cleaning system**
We estimated the number of thin wafers going through temporary bonding to be > 10M in 2017. This would be ~8% of the TOTAL number of thin wafers.
Ratio Bonded Thin Wafer vs. Total Thin Wafer

- Graph below shows the relative ratio between the total number of thin wafers and the number of temporary-bonded thin wafers.

**Ratio Bonded vs. TOTAL thin wafers**

<table>
<thead>
<tr>
<th>Year</th>
<th>Ratio Bonded vs. TOTAL thin wafers</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>4%</td>
</tr>
<tr>
<td>2012</td>
<td>4%</td>
</tr>
<tr>
<td>2013</td>
<td>5%</td>
</tr>
<tr>
<td>2014</td>
<td>5%</td>
</tr>
<tr>
<td>2015</td>
<td>5%</td>
</tr>
<tr>
<td>2016</td>
<td>7%</td>
</tr>
<tr>
<td>2017</td>
<td>8%</td>
</tr>
</tbody>
</table>
Temporary Bonder and Debonder Market

CAGR is 37%

<table>
<thead>
<tr>
<th>Year</th>
<th>Temporary Bonder and Debonder Market Value (US$M)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>$39</td>
</tr>
<tr>
<td>2012</td>
<td>$44</td>
</tr>
<tr>
<td>2013</td>
<td>$56</td>
</tr>
<tr>
<td>2014</td>
<td>$88</td>
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<tr>
<td>2015</td>
<td>$115</td>
</tr>
<tr>
<td>2016</td>
<td>$195</td>
</tr>
<tr>
<td>2017</td>
<td>$261</td>
</tr>
</tbody>
</table>
Final Conclusion

• As chips get thinner and wafer diameter increases, thinning/handling procedures are required.

• Temporary bonding equipment is still a small market today but it is expected to grow as needs for thin wafer handling grows.

• Power and 3D ICs applications are currently driving this market.

• We believe 3D ICs will then become the predominant application for temporary bonders > 2015.
Thank you